

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
29 January 2004 (29.01.2004)

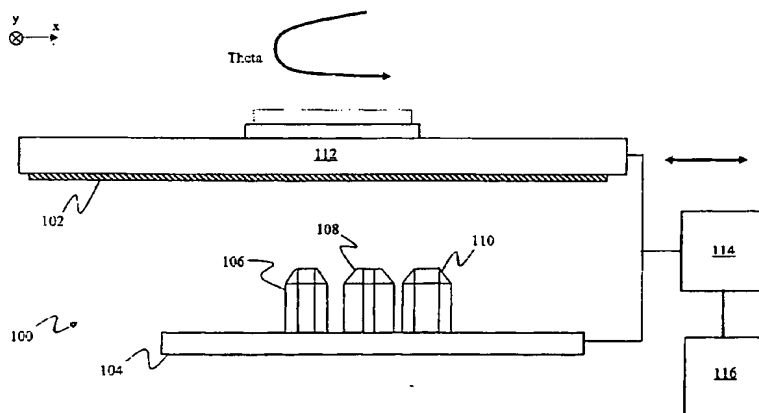
PCT

(10) International Publication Number
WO 2004/010477 A2

- (51) International Patent Classification⁷: **H01L**
Fremont, CA 94538 (US). YU, Chaw-Chi [US/US]:
20625 Reid Lane, Saratoga, CA 95070 (US).
- (21) International Application Number:
PCT/US2003/022928
- (74) Agents: YIM, Peter, J. et al.; Morrison & Foerster LLP.
425 Market Street, San Francisco, CA 94105-2482 (US).
- (22) International Filing Date: 22 July 2003 (22.07.2003)
- (81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CIL, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, IIR, IU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
60/397,941 22 July 2002 (22.07.2002) US
60/403,996 17 August 2002 (17.08.2002) US
- (71) Applicant (*for all designated States except US*): ACM RESEARCH, INC. [US/US]; 46520 Fremont Boulevard, Suite 610, Fremont, CA 94538 (US).
- (72) Inventors; and
- (75) Inventors/Applicants (*for US only*): WANG, Hui [US/US]; 340 Jacaranda Drive, Fremont, CA 94539 (US). AFNAN, Muhammed [US/US]; 1048 Vuelta Olives, Fremont, CA 94539 (US). YIH, Peihaur [—/US]; 37171 Sycamore Street, #824, Newark, CA 94560 (US). KOEHLER, Damon, L. [US/US]; 39601 Fremont Blvd.,
- (84) Designated States (*regional*): ARIPO patent (GI, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).
- Published:
— without international search report and to be republished upon receipt of that report

[Continued on next page]

(54) Title: ADAPTIVE ELECTROPOLISHING USING THICKNESS MEASUREMENTS AND REMOVAL OF BARRIER AND SACRIFICIAL LAYERS



(57) Abstract: A metal layer formed on a semiconductor wafer is adaptively electropolished. A portion of the metal layer is electropolished, where portions of the metal layer are electropolished separately. Before electropolishing the portion, a thickness measurement of the portion of the metal layer to be electropolished is determined. The amount that the portion is to be electropolished is adjusted based on the thickness measurement. A metal layer formed on a semiconductor wafer is polished, where the metal layer is formed on a barrier layer, which is formed on a dielectric layer having a recessed area and a non-recessed area, and where the metal layer covers the recessed area and the non-recessed areas of the dielectric layer. The metal layer is polished to remove the metal layer covering the non-recessed area. The metal layer in the recessed area is polished to a height below the non-recessed area, where the height is equal to or greater than a thickness of the barrier layer.